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DATA PROCESSOR (RPV).(U)
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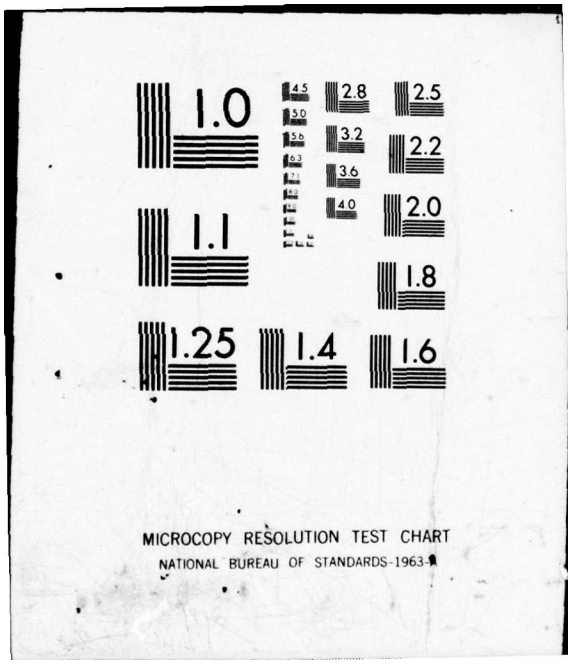
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1.25
1.4
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1.8
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2.8
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5.0
5.6
6.3
7.1
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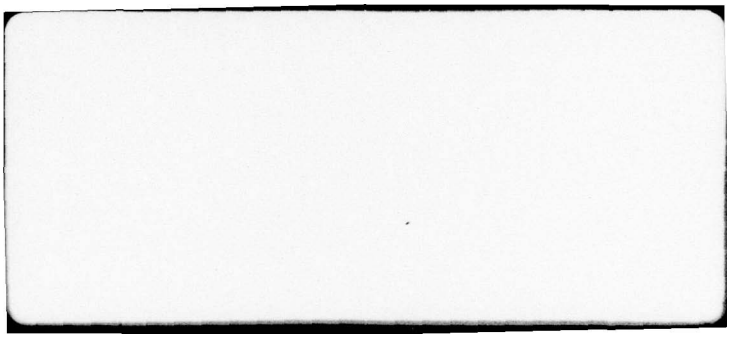

FAIRCHILD IMAGING SYSTEMS
A Division of Fairchild Camera and Instrument Corporation

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REPORT NO. ED-AX-80

6 DATA PROCESSOR (RPV)

9 FINAL REPORT.

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A. Roberts, Program Manager

I. Hirschberg, Director

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FAIRCHILD IMAGING SYSTEMS
A Division of Fairchild Camera and Instrument Corporation

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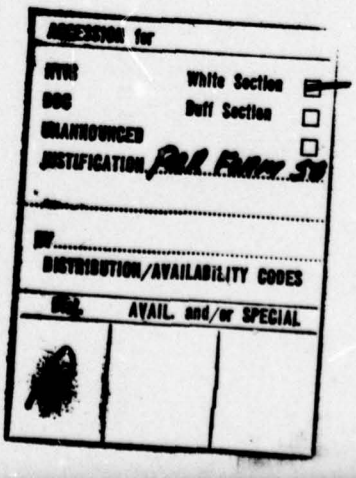


LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

This report describes a program for the development, brassboard fabrication and testing of an airborne Solid State CCD Data Processor that demonstrates a method of transmitting a standard TV signal over a narrow bandwidth link by processing the TV signal, using CCD-488 devices in an "analog storage mode". The Data Processor brassboard shown in Figure 1, is designed to electrically interface with the Systems Research Laboratory's (SRL) TV Camera, 326-H2 and the Fairchild CCD-488 TV Camera (MV301) and to mechanically interface with the Aquila air frame.

The transmitted signal from the electronic camera/data processor system is received at a ground station where the imagery is reconstructed utilizing two tube scan converters for image storage. The reconstructed video is displayed on a standard TV monitor.

A major component in the system is the Fairchild CCD-488. The Fairchild CCD-488 is a solid state photosensitive device that functions on the "charge-coupled" principle and is primarily used as an imaging television sensor (CCD operation as an imager is described in detail in Appendix A). The CCD-488 device also has provisions to accept input data in electrical form. It is this mode of operation that is applicable to the Solid State CCD Image Processor.

The CCD-488 analog storage array (CCD operation as a storage device is described in detail in Appendix C) consists of 380 columns of storage registers with each column storing 244 analog levels. An input register is located along the top of the array, with an output register along the bottom edge. An array is thus capable of storing one field of TV video and a pair of arrays stores a complete frame of interlaced TV video. The video signal is transferred into the array at standard

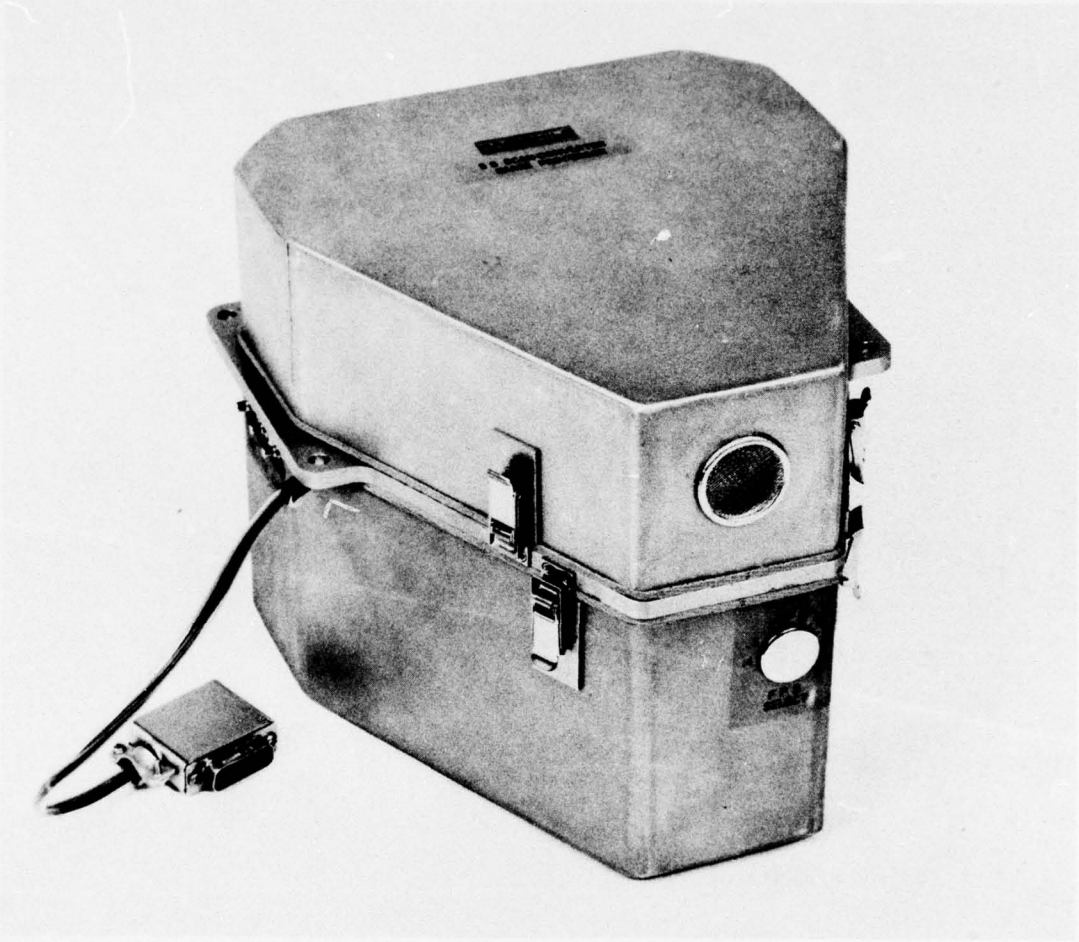


FIGURE 1. RPV DATA PROCESSOR

77P57

TV scan rates and is read out selectively at the same rate or a much slower rate. A pair of arrays thereby provides the storage capacity to accept one frame of TV video from a TV camera operating at standard TV rates and read that same frame out at a much slower rate to reduce the bandwidth of the video signal.

2.0 TEST RESULTS

The RPV Data Processor program successfully demonstrated the method of reducing the bandwidth of standard TV signals by uniquely processing the signal using CCD-488 devices in an analog storage mode. The results of the test performed at Fairchild are documented in pages 4 and 5. It should be noted that a horizontal resolution of 250 TV lines/picture height was obtained with 285 TV lines as the limiting resolution of the CCD. This reduced performance is attributed to the transfer efficiency (30%) of the camera at the Nyquist limit of the CCD. 250 TV lines/picture height was the vertical resolution of the camera under the test condition and this reflected in the resulting vertical data. Subsequent testing (re-alignment of the camera beam current) resulted in 488 TVL/PH resolution in the vertical direction. This is the limiting resolution of the CCD.

2.1 IMAGE QUALITY

The test results highlighted the following parameters which effect the image quality from the processor. They are:

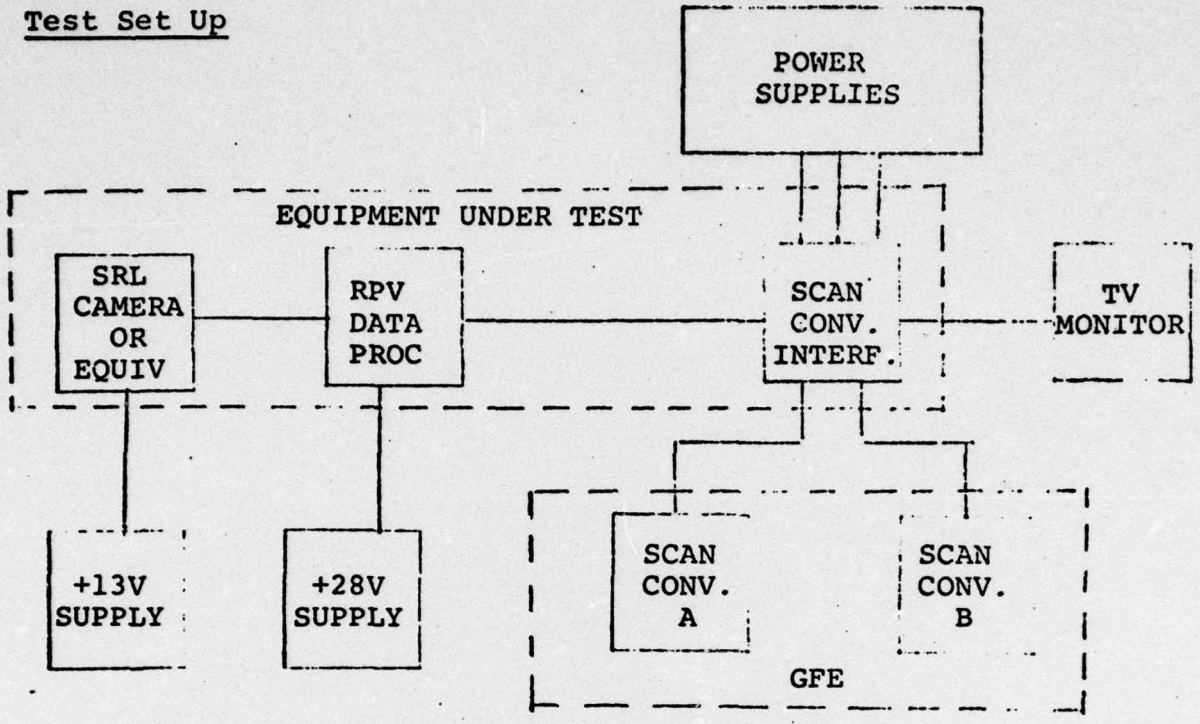
- Vertical signature
- Single pixel blemishes
- Average dark current
- Mismatch between the array video outputs

a) Vertical signature appears as vertical streaking superimposed over the image. It appears to be inherent in the CCD when used in the storage mode. The primary causes of this condition is under investigation.

b) Single pixel blemishes appear as single element white dots in the picture. This condition is caused by dark current spikes in the CCD. The number of single pixel blemishes appearing in the image is a function of the quality of the array and of the array temperature.

ACCEPTANCE TEST: RPV DATA PROCESSOR

1. Test Set Up



2. Test Data

2.1 Resolution (Room Light)

Frame Rate (FPS)	Horiz.	Vert.
7.5	250 TVL/PH	250 TVL/PH
4	250	250
2	250	250
1	250	250

2.2 Hold Mode

Initiate hold, picture will not update until released. ✓

2.3 Video Bypass

Initiate bypass, standard video is transmitted. ✓

3. Equipment

CCD 488 Resolution Chart
TV Monitor
2 GFE Scan Converters

Tested by: A. Roberts 2/17/77
DATE

Witnessed by: [signature] 2/17/77
DATE

c) Average dark current manifests itself in the saturation of the image, beginning at the bottom of the picture (longest stored lines) and decreasing towards the top. It is most severe at the low scan rates. Cooling of the CCD's effectively eliminates this problem.

d) The mismatch in array outputs effect the quality of the image in two major areas, black level and dynamic range. Both conditions are inherent in the devices, but may be compensated for through external circuitry.

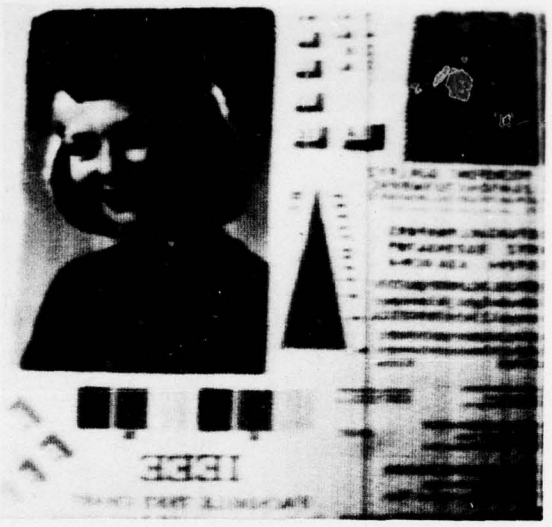
2.2 GROUND STATION PERFORMANCE

The RPV Ground Station performed its design function with the following limitations:

a) A momentary loss of sync during data update.
b) A shift in the picture position between scan converters.
c) 60Hz crosstalk between scan converters.
d) The need for repeated adjustment of the scan converter gain and background level.
e) An inherent difference in the picture intensity and background between scan converter displays.

2.3 IMAGERY EXAMPLES

Typical imagery from the RPV Data Processor System at the Ground Station output is shown in Figure 2.



IMAGERY IS INVERTED THROUGH SYSTEM'S OPTICS

FIGURE 2. TYPICAL IMAGERY AT THE GROUND STATION OUTPUT

3.0 DESIGN

3.1 AIRBORNE ELECTRONICS

The RPV Data Processor Airborne Electronics converts EIA RS170 Video to non-interlaced slow scan video at any one of six selectable frame rates; .35, .5, 1.0, 2.0, 4.5, 7.5 FPS.

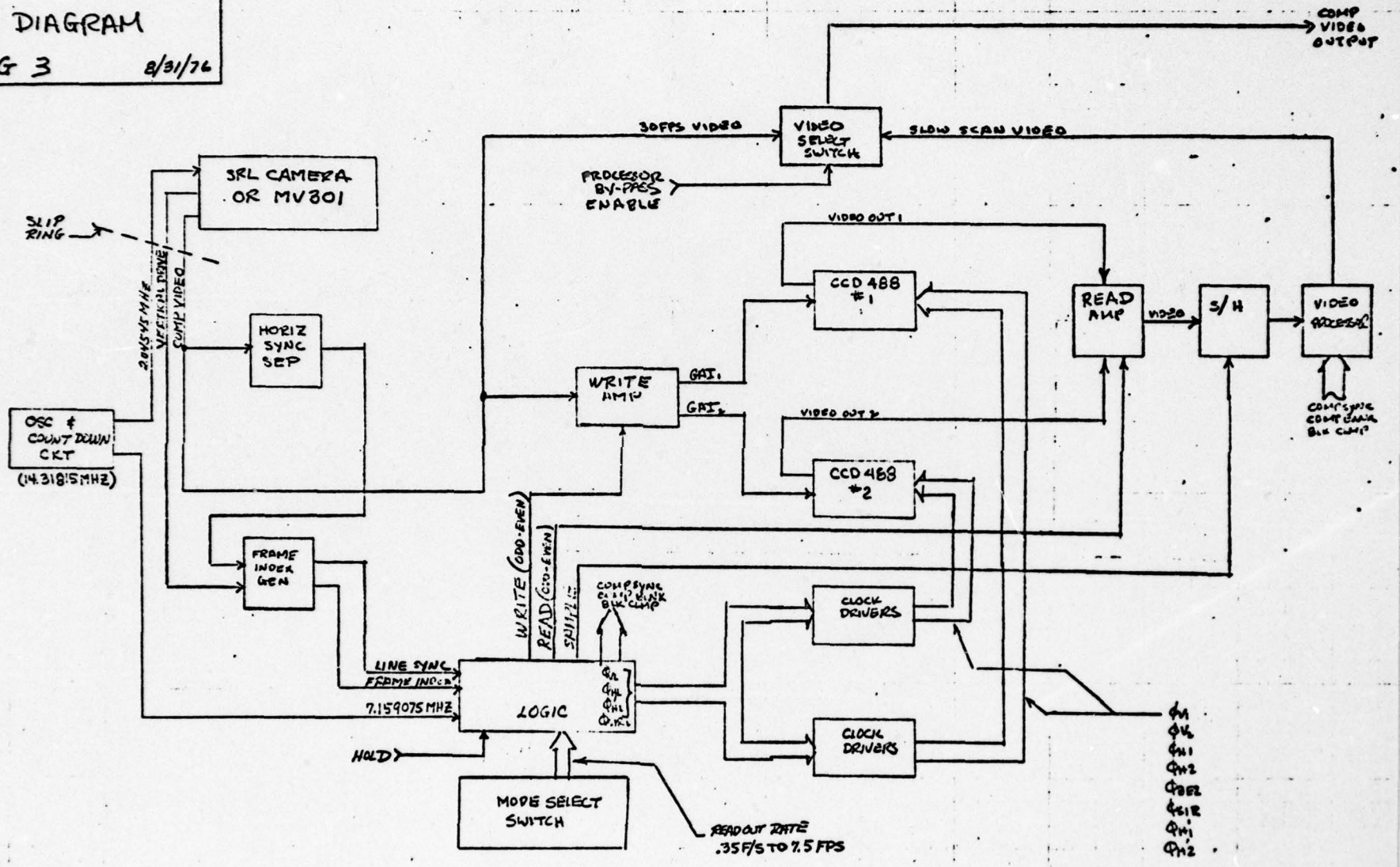
The functional block diagram of the Airborne Electronics is shown in Figure 3. The interface camera (SRL 326-H2 or Fairchild MV301) is externally synchronized to the PRV Data Processor via a common master clock. Composite video and the Vertical Drive pulse are outputted from the interface camera and used in the processor to derive line and frame sync information in addition to primary video. The sync separator and frame index generator circuits are contained on the Write Amplifier. A timing diagram describing the performance of this circuit is shown in Appendix B (TD-3). These functions are accomplished using low power CMOS "One-Shots".

3.1.1 Logic System

The logic system is divided into three wire wrap boards. To minimize the total power dissipation, a mix of CMOS and TTL logic elements are used. TTL is used where the switching rates exceed the limits of the CMOS devices. The wire wrap boards are partitioned by function and device type as follows:

6127-100SD1,	SHT 1 Control Logic	CMOS
,	SHT 2 Write Logic, Frame	"
6127-100SD2,	Write Logic, Line	TTL
	Combining Logic	"
6127-100SD3,	SHT 1 Read Logic, Line	CMOS
,	SHT 2 " " , Frame	"
,	SHT 3 CP_{read} Generator	"

RPV DATA PROCESSOR
AIRBORNE PACKAGE
BLOCK DIAGRAM
FIG 3 8/31/76



The Control Logic sets the desired read, write and prime cycles by counting frame index pulses from the frame index generator. The count is preset by programming the decode logic with a six position wafer switch. Each cycle consists of a 1/30 sec prime period, during which the storage array is cleared, a 1/30 sec write period, a variable read period and four 1/30 sec sync periods, which allows the ground station to prepare for the next frame of video. In addition, a hold mode is provided which allows the retention of the last written frame until the hold is released. The Control cycle timing is shown in Appendix B (TD-1).

The Write Logic generates the necessary CCD clock wave forms for inputing data into the storage arrays. The line circuit uses the master clock to derive the bit rate and line transfer intervals. The bit rate for writing is 7.159MHZ. The 2.54MHZ for the interface camera and the read logic is derived here.

The frame logic synchronizes the write sequence so that the odd/even fields are read into the storage arrays in the proper order. The Write Logic timing is shown in Appendix B (TD-2).

The Read Logic generates the necessary CCD clock wave forms for outputting data from the storage arrays and sync and blanking intervals for the composite slow scan video output. The line circuit uses the clock pulse generated in the CP_{read} generator to derive the bit rate, line transfer and sync and blanking intervals. The bit rate is one of six selectable frequencies derived from the master clock. Frequency selection is made through a 3-bit digitally encoded signal and a 6-input multiplexer. The video enable gates generated here provide the proper sequencing of data transfer from the storage arrays to provide a non-interlaced output. The frame logic generates the basic 525-line format for the slow scan output. Timing diagrams of the line read logic is shown in TD-3. The Read, Write and Prime wave forms are combined in the SD2 board. Timing diagrams of the combined logic are shown in Appendix B(TD-4).

3.1.2 Write Amplifier

Video information from the interface camera is conditioned in the Write Amplifier board (6127-100 SD4) for inputting to the storage arrays. Odd field data is inputted to one storage array while even field data to the other. The circuit is comprised of integrated circuit amplifiers, transistors and discrete components and is contained on a semi-circular hard-wired board.

3.1.3 Read Amplifier

Slow Scan Video data outputted from the storage arrays is processed in the Read Amp (6127-100 SD5). The read amplifier contains a sample and hold circuit and the necessary processing for the generation of composite video. Alternate lines from the two storage arrays are combined thus providing a non-interlaced output for the data link. Where standard video is the desired output, a video select relay is provided to allow the bypassing of the data processor. The relay is energized by an external command. The circuit is comprised of integrated circuits amplifiers, transistors and discrete components and is a semicircular hard-wired board.

The storage CCD arrays are contained on a hard-wired rectangular-shaped board (6127-100SD6,7) along with the hybrid drivers and regulators. Thermo-electric coolers for each array along with the necessary heat sink are attached.

3.1.4 Power Supplies

The Processor Electronics is powered by ±12VDC and +5VDC as derived from three DC-DC converters. The converters operate from +28VDC and require a total input power of 12.8W.

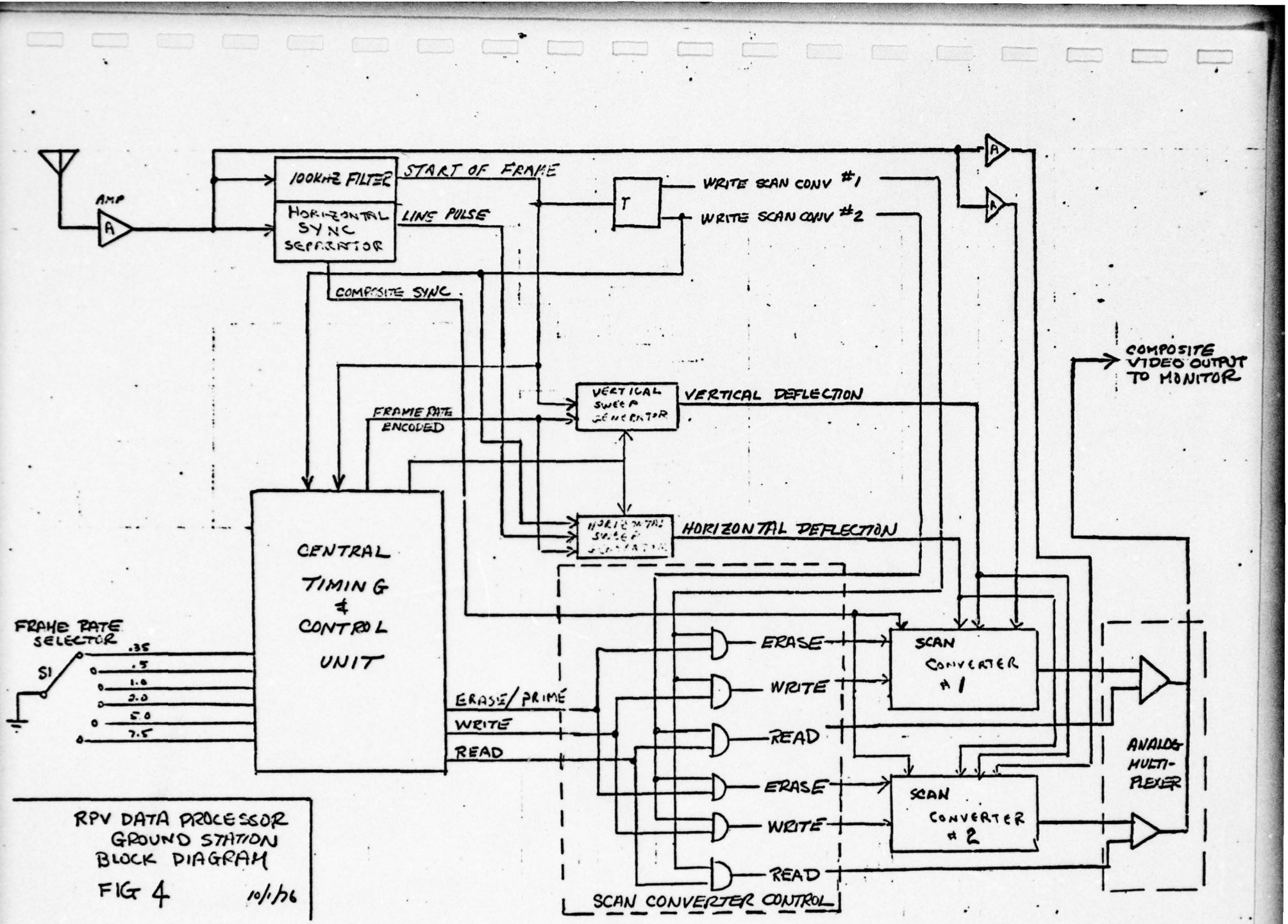
The Thermoelectric coolers are powered by +5VDC as derived from two DC-DC converters. The converters operate from +28VDC and require a total input power of 12.4W (6.2W/cooler).

3.2 GROUND STATION

The ground station consists of a standard 525-line television monitor, two Hughes Scan Converters which write data at one of six slow scan data rates and the logic and electronics to receive the video signal and control the ground station operation. The two scan converters operate in a ping-pong fashion, that is, data is written into one scan converter while it is read from the other and vice versa. The functional block diagram is shown in Figure 4.

The transmitted video format consists of a 100 KHz burst at the start of each transmitted frame. This serves as a synchronizing pulse (equivalent to vertical sync) to identify the beginning of each frame of slow scan data. This interval occurs at the beginning of a 2/30 second time interval (2 frame times) during which the airborne camera system is preparing the next frame for transmission. This 2-frame fixed time period is then followed by 37 blank video lines at the pre-selected slow scan data rate. At the end of the 37 line period, 488 lines of conventional video are transmitted at the slow scan rate. At the conclusion of video data, four 1/30 (four frame times) second interval is inserted before the next frame identification burst. The timing sequence for the ground station is shown in Appendix B (Timing Diagram TD-5).

The POWER ON sequence in the ground system causes a prime and erase command to be generated for each scan converter. The ground station then arbitrarily selects one of the scan converters to be selected for the initial write operation. When the frame ID burst is detected (via a dedicated low pass filter) the write logic is activated and initialized. The scan converters is placed in the write mode. When horizontal blanking pulses are detected by the receiver, the first 37 such pulses are counted and stripped from the incoming video. At the completion of 37 lines, the



RPV DATA PROCESSOR
GROUND STATION
BLOCK DIAGRAM

FIG 4 10/1/76

vertical and horizontal sweep generators are enabled and the incoming video is written on the selected scan converter. The slop of the horizontal and vertical sweeps are controlled by a switch which selects one of six slow scan rates. When 488 lines are written (counted) the scan converter enters a read mode, and data is read at a conventional 30 frame per second 2:1 interlaced rate. The picture, so stored, is read continuously at 30 fps until a new picture has been received and written on the other scan converter. At such time, the other scan converter is selected for display and the operation continues.

The two scan converter read cycles (conventional 30 fps) are synchronized by a master-slave relationship. The composite sync generated by the master is used to control the sweeps in the unit designated as the slave. In this way, undesirable effects of switching from one unit to the other are eliminated.

At the conclusion of writing the 525th Video line on one scan converter, it is placed in the read mode. At the same time a "prime and erase" command are generated to the other converter. This prime and erase operation requires 11 field cycles (at the thirty frame per second rate). The prime/erase function results in a more uniform black than the erasing function alone. The operation begins immediately after the 525th line is written on the other converter. The 11 required field times are the 1/30 second interval before the next frame ID burst (used to sync) and the 2/30 second interval that occurs from the ID burst to the start of data.

The addition of eleven TV fields,or six TV frames at 30 fps, to allow for the scan converter prime/erase cycle modifies the frame update rate such that it is different than the actual frame rate of the slow scan video. The data rate or

element rate is not effected by this modification. Table 1 shows the relationship between the Actual Frame Rate, Frame Update Rate, and Data Rate of the slow scan video output.

The only additional feature in the ground station is a "HOLD" mode. When this command occurs (the command is generated in the ground station) the ground station enters the hold mode at the conclusion of writing a slow scan frame. The normal prime and erase functions occur on the other scan converter but the receiver does not look for an ID burst (none will be forthcoming). Rather, the ground station waits for a "reset hold" command which serves the same purpose as the ID burst. It then waits for horizontal sync pulses, removes 37 lines, and continues in a normal mode.

3.3 INTERLACE/NON-INTERLACE OPTION

The system design, as presented, does not include an interlaced/non-interlaced option for the slow scan rate output data. The decision to drop the interlaced slow scan readout option is based on the difficulty in precisely formating two fields at slow scan rates in the ground station scan converters.

At slow scan rates (.5,1.0 etc., FPS), data obtained during the odd field write interval must precisely interlace with data written as long as 1.5 seconds earlier. Any change due to such anomalies as 60Hz modulation will result in line pairing. In addition, the purpose of interlacing is to reduce monitor flicker. This problem is not applicable to the slow scan rate readout because this data is not monitor-displayed. Only the scan converters readouts in the ground station are displayed and this data is interlaced.

Finally, the degree of complexity to implement both options is considered unwarranted based on the consideration discussed.

TABLE 1

SELECTOR SW INDICATOR POSITION (FPS)	ACUTAL FRAME RATE (FPS)	FRAME UPDATE RATE (FPS)	DATA RATE (ELEMENT RATE) MHZ
7.5	7.5	3.0	1.790
4	4.286	2.31	1.023
2	2.143	1.5	0.511
1	1.071	0.882	0.256
.5	.536	0.484	0.128
.4	.357	0.333	0.085

3.4 CAMERA INTERFACE

3.4.1 SRL Camera

The SRL camera purchased as part of this program requires that the clock pulse be turned on after power is applied to the camera. After being apprised of this condition, SRL proposed a circuit which delayed transfer of the clock until the power to the camera stabilized. This circuit has been incorporated into the processor and has been shown to perform satisfactorily.

3.4.2 MV 301 CCD Camera

Compatibility testing of the processor with the MV 301 camera has been satisfactorily performed. The results show that the MV 301 does not require an external clock since both equipments are in synchronism through TV line and frame syncs as derived from crystal oscillators in the MV 301 camera. Some 120 Hz interference did result in low light level scenes. This condition should be evaluated in the final test installation.

3.5 MECHANICAL

3.5.1 Volume

The three wire wrap boards, two semi-circular hard-wired boards, one CCD array board and five DC-DC Converters are contained within the outline dimensions of the Mini Pan Camera, as shown in Figure 5 and Figure 6. Dwg 6127-100L2 is a detailed layout of the processor utilizing all additional space alloted during the installation study at Lockheed. Access to the rotary switch for mode changes is made through an access hole on the underside of the package beneath the skin line of the RPV. The electronics is accessible by removing two covers on either side of the package.

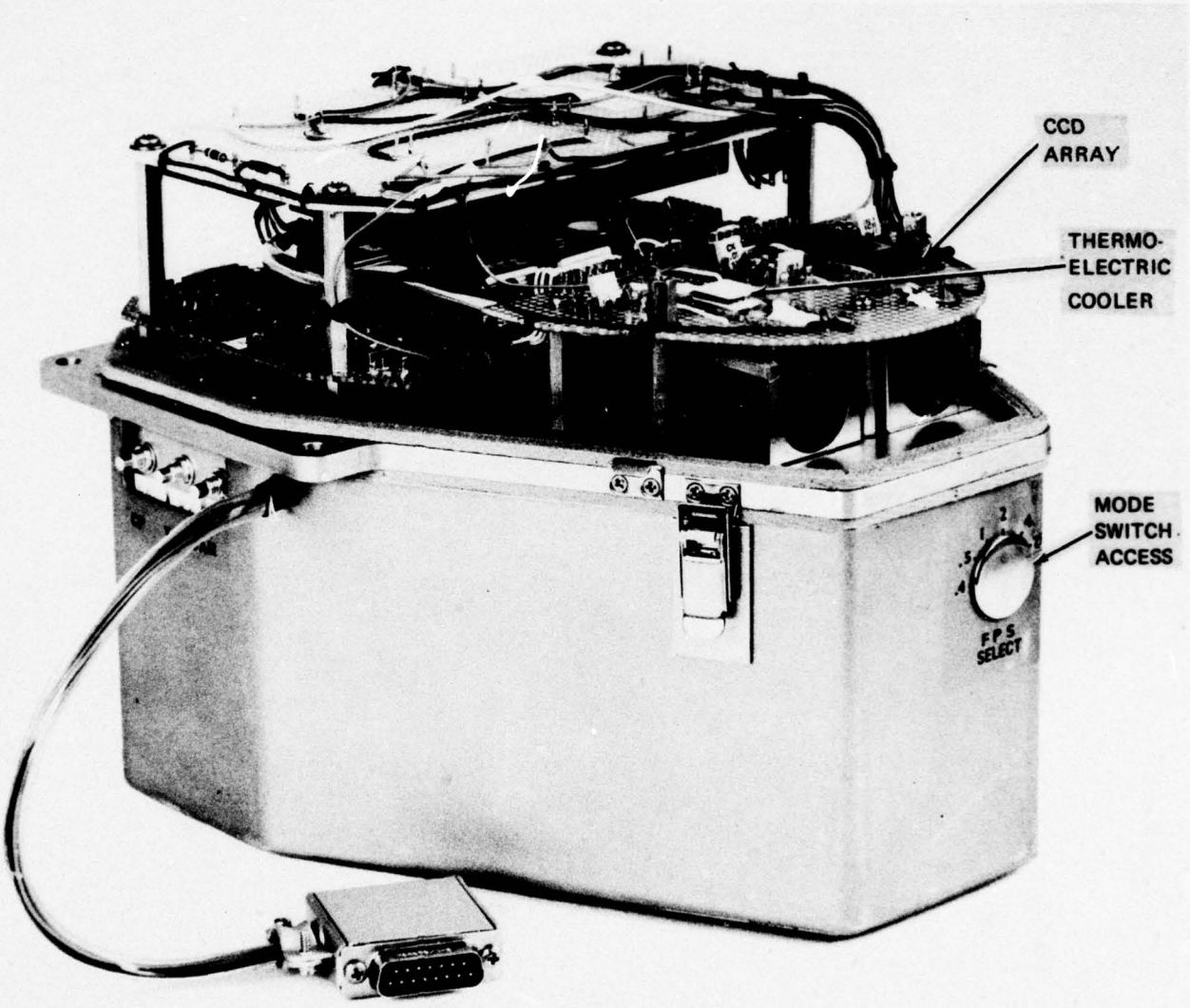


FIGURE 5. RPV DATA PROCESSOR CCD ARRAY AND ASSOCIATES ELECTRONICS

77P60

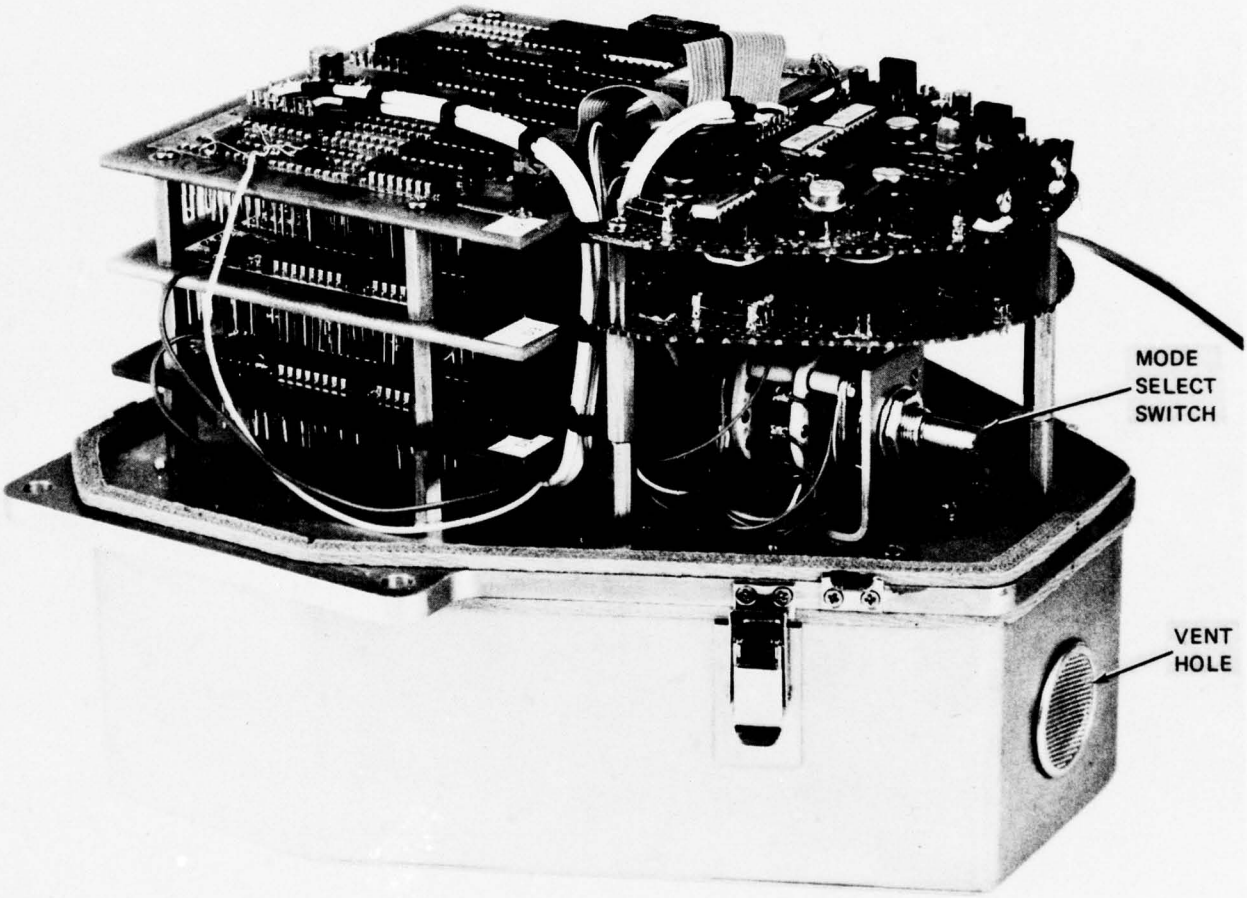


FIGURE 6. RPV DATA PROCESSOR LOGIC AND PROCESSING ELECTRONICS

3.5.2 Cabling

The system cabling diagram is shown in Figure 7.

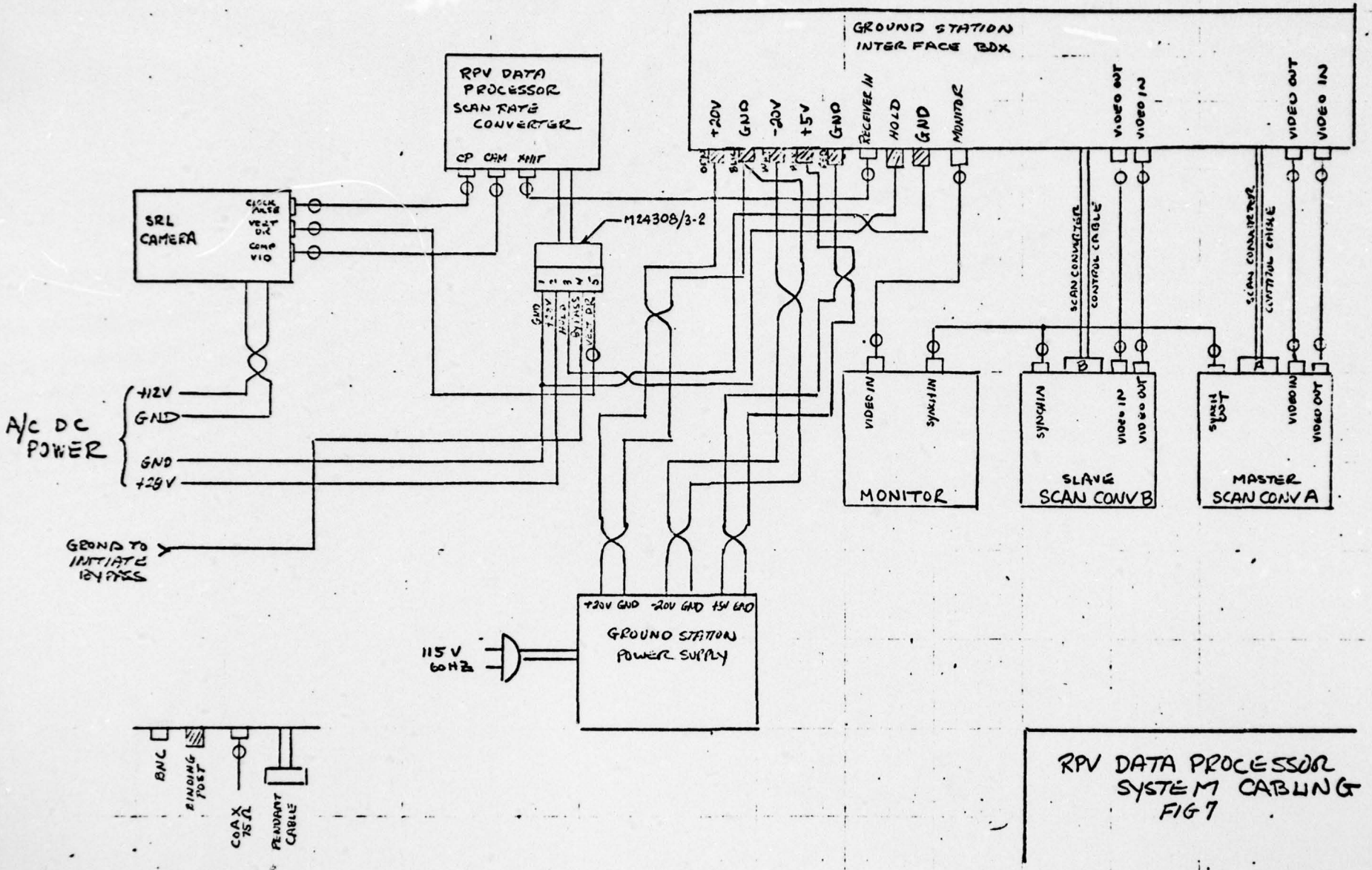
3.5.3 Parts Count

The following is the parts count for the Airborne Electronics:

	QTY
Logic TTL	18
Logic CMOS	60
IC's Analog	7
Hybrid drivers	8
IC Regulators	16
DC-DC Convertors	5
Relays	1
Switch	2
Transistors	21
Diodes	10
Resistors	129
Capacitors	113
Inductors	1
CCD Arrays	2
TE Coolers	2
Crystal OSC	1

3.5.4 Weight

The Airborne Package weighs 8 lbs.



RPV DATA PROCESSOR
SYSTEM CABLING
FIG 7

A P P E N D I X "A"

Appendix A

Charge - Coupled Image Sensor

Charge-coupled image sensors integrate photon-generated minority carriers in depletion wells formed by the application of a bias voltage to elements of a control electrode (gate) structure overlaying photo-sensitive regions of the substrate. Following an integration period, the carriers are transported as individual signal packets by potential well motions induced by clocking the gate electrodes. After a sequence of transport steps determined by device organization, signal packets corresponding to element rows are serially shifted to an on-chip detector for conversion to an output video signal.

The cell organization of a CCD and the number of charge transport gates (phase lines) per cell, are of concern to the camera designer since precisely timed gate drive waveforms must be supplied to the device for self-scan operation. The interline-transfer (ILT) organization is used exclusively for the Fairchild family of area array CCD's, which includes designs with 100 x 100, 190 x 244 and 380 x 488 elements. These designs employ two-phase (2Ø) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, these designs all utilize buried-channel charge transport principles. In a buried-channel CCD, the signal carries are kept away from the silicon surface by an electrical field associated with an implanted layer of ions. Thus the trapping of carriers by surface states is inhibited resulting in high charge-transfer efficiencies which are essentially independent of the signal

charge magnitude. For the 190 x 244 and 380 x 488 designs, buried-channel operation has been combined with on-chip low-noise floating-gate amplifiers. The combination of features extends the CCD performance range to threshold signal levels of a few tens of electrons per depletion well.

Figure 1 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site which is one-half stage of a 2Ø vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate ($\emptyset_p$) is LOW and the adjacent transfer gate ($\emptyset_{V1}$) or $\emptyset_{V2}$) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing $\emptyset_p$ LOW during each vertical blanking interval and applying complementary $\emptyset_{V1}$, $\emptyset_{V2}$ waveforms with HIGH states during alternate V-blanking periods.

At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent $\emptyset_{V1}$ sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into $\emptyset_{V2}$ sites. row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding $\emptyset_{V1}$ LOW and $\emptyset_{H1}$ HIGH during the horizontal

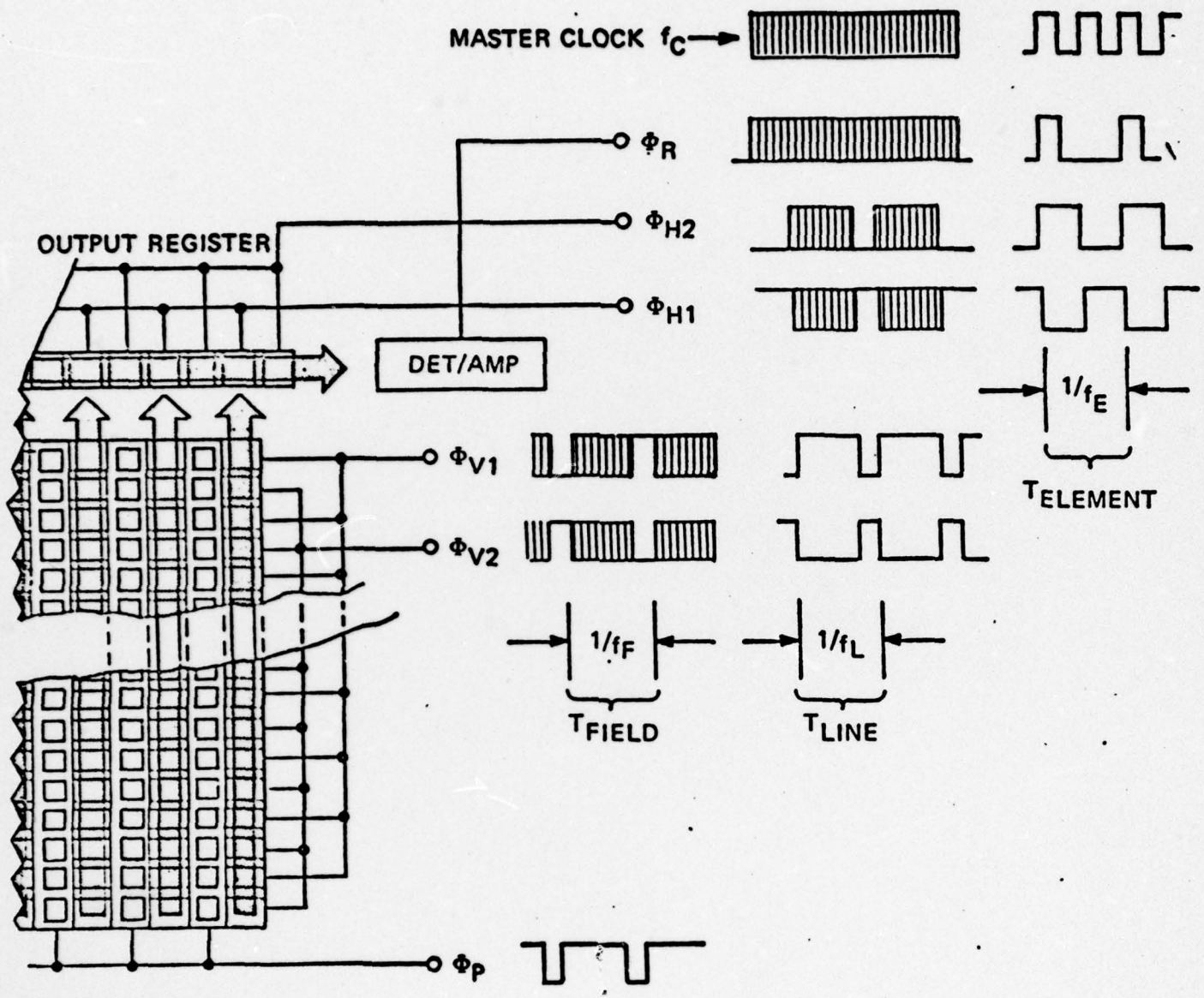


FIGURE 1

INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORMS

75-1030

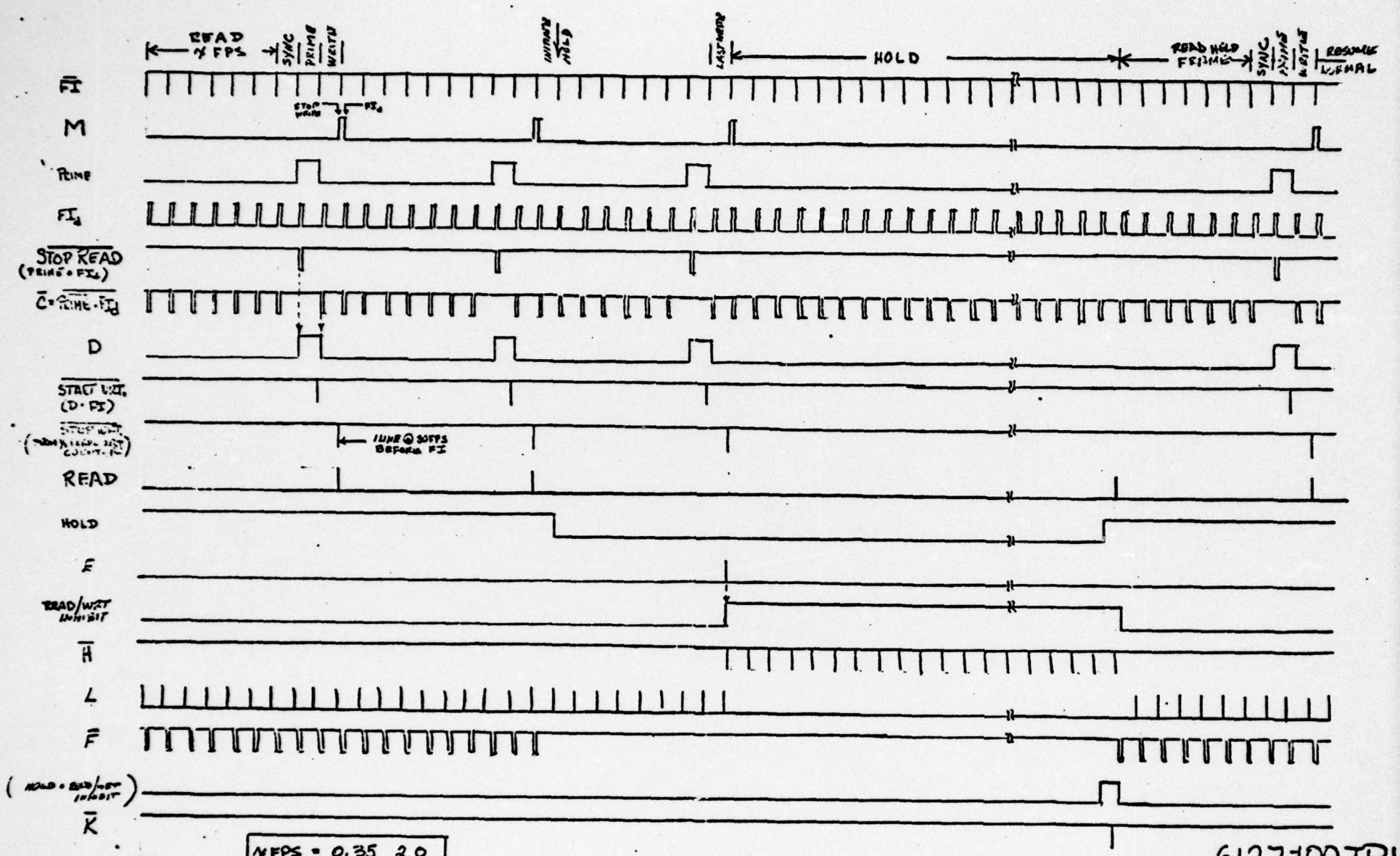
blanking interval. Complementary square-wave pulses at element rate are applied to the $\emptyset_{H1}$, $\emptyset_{H2}$ transport gates to serially shift packets to the output detector.

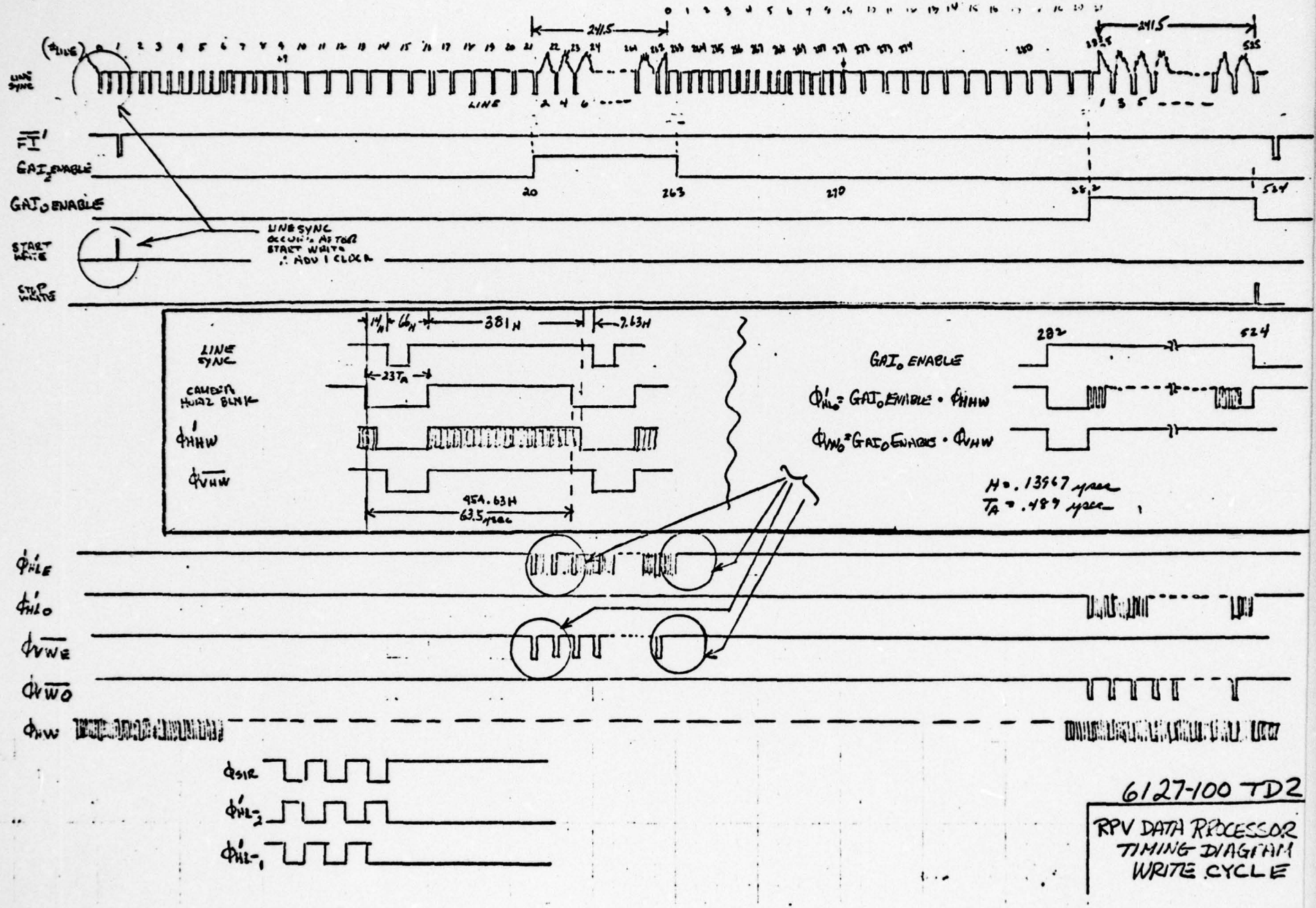
A P P E N D I X "B"

D R A W I N G S

List of Drawings

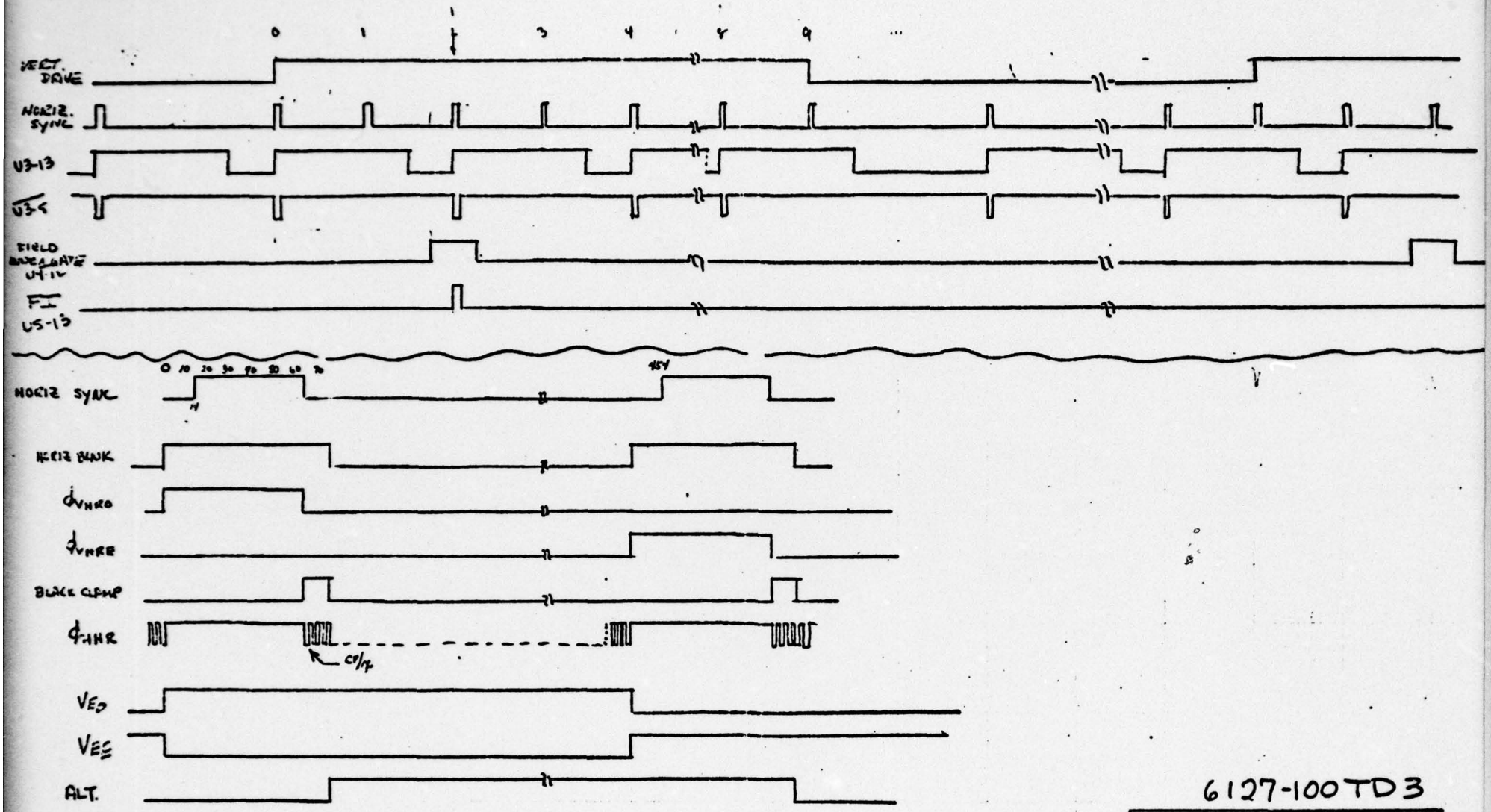
6127-100	SD1	Schematic:	Control/White Logic Frame
	SD2		Write Logic Line
	SD3		Read Logic/CP$_{read\ Gen}$
	SD4		Write Amplifier
	SD5		
	SD6		Clock Driver/Array
	SD7		Regulator Assy
	SD8		SC Playback CKTS, Ground Station
	SD9		Sweep Generator " "
	SD10		Logic, Ground Station
	SD11		Video Processor, Ground Station
	TD1	Timing Diagram:	Airborne Control Cycle
	2		Airborne Write Cycle
	3		Airborne READ/Frame Index
	4		Airborne COMBINED
	5		Ground Station
	CD1	Interconnecting Wiring, Airborne Package	
	CD2	" " , Ground Station	
	L2	Layout drawing, Airborne Package	
	L1	Preliminary Volume Study	


READ N FPS
SYNC
PRIME
WRITE
HOLD
READ HOLD
RESUME NORMAL
FI
M
PRIME
STOP READ
HOLD
READ
E
L
F
K
N FPS = 0.35 2.0
0.5 5.0
1.0 7.5
6127100TD1
RPV DATA PROCESSOR
TIMING DIAGRAM
CONTROL CYCLE



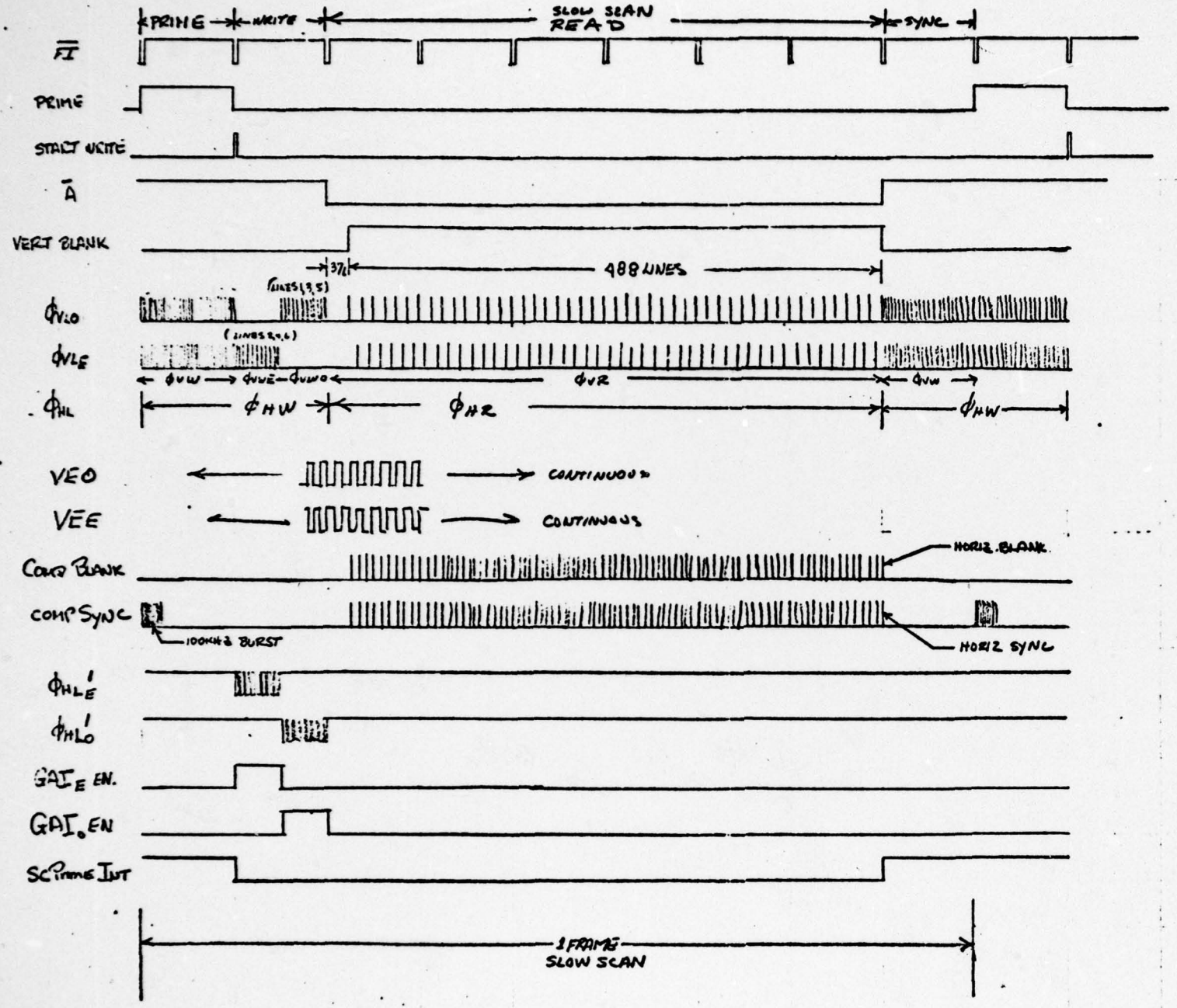
6127-100 TD2

RPV DATA PROCESSOR TIMING DIAGRAM WRITE CYCLE



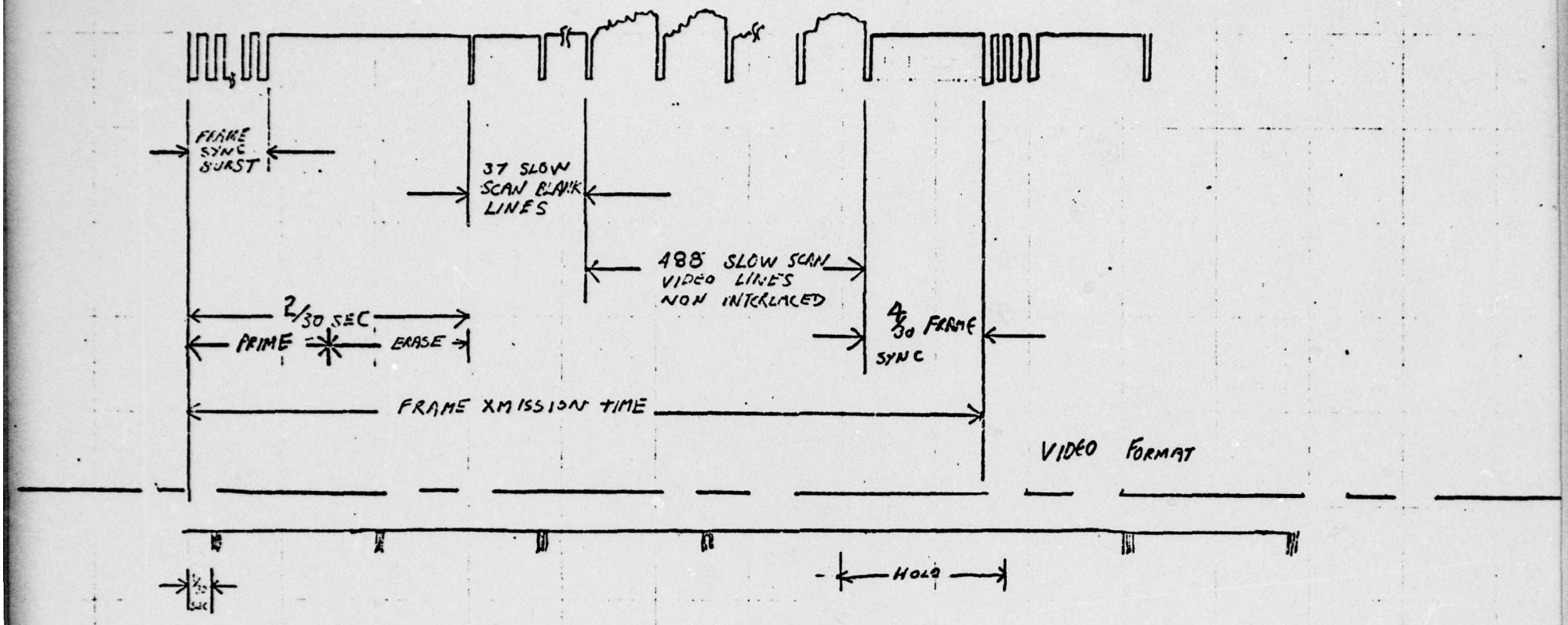
6127-100TD3

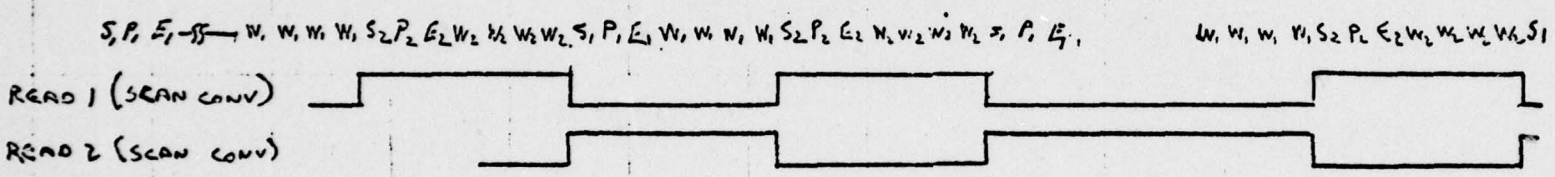
RPV DATA PROCESSOR
TIMING DIAGRAM
READ CYCLE
&
FRAME INDEX



6127-100 TD4

RPV DATA PROCESSOR
TIMING DIAGRAM
COMBINED LOGIC





S SYNC
P PRIME
E ERASE
W WRITE

6127-100TD5

RPV DATA PROCESSOR TIMING DIAGRAM GROUND STATION CONTROL CYCLE

A P P E N D I X "C"

Appendix C

Charge - Coupled Storage Device

The 488 CCD array, when used in a storage mode is a 92,720 bit analog shift register that can be used in analog signal processing applications that include delay and temporary storage of analog information.

The device is organized in a series-parallel-series configuration (SPS). Electrical information in voltage form is applied to an input charge injection port which samples the input and generates proportional charge packets in a 380 element serial input register. The information is then transferred in parallel to registers that transport the packets to a 380 element serial output register. Clocking of the output register then delivers the charge packets to an on-chip amplifier that delivers at the output corresponding analog voltage levels. Continuous clocking of the device reproduces at the output a line-by-line representation of 380 elements each of the input information.

Functional Description

The 488 CCD storage device consists of the following subsections:

1. A charge injection port that accepts the input electrical information and converts it to proportional charge packets.
2. A 380 element long serial input register coupled to the charge injection port.
3. Three hundred and eighty parallel registers each 244 elements long that transport the charge from the serial input register to the serial output register.
4. A 380 element long serial output register coupled to an output amplifier.
5. A two stage floating gate output preamplifier which detects and converts the charges delivered from the serial output register to the output terminal V_{OUT}.

Charge Injection Port

The charge injection port consists of an input source which supplies electrons to the input register, modulated by the voltage (V_{IN}) on the analog input gate. In operation, the input source driven by clock $\emptyset_{SIR}$ injects charge under the analog input gate V_{IN}. The charge retained under V_{IN} will be proportional to the analog voltage. The excess charge will flow back to the $\emptyset_{SIR}$ terminal when it changes state. The charge packet under V_I is then transferred to the input register when $\emptyset_{H2}$, goes HIGH.
The clock $\emptyset_{SIR}$ is called the input sampling clock. This clock frequency should be selected to be more than twice the input bandwidth signal at V_{IN} for proper reconstruction of the analog waveform at the output. The input V_{IN} is typically biased around .5 volts and a swing of 0.5V from this dc bias can be obtained.

Serial Input Register

The input register is a 380 element 2 phase analog transport register which transfers the charge packets generated by the charge injection ports into the parallel registers. Charge packets are moved serially into the register by clocking $\emptyset_{H1}$, and $\emptyset_{H2}$, which are of the same frequency as $\emptyset_{SIR}$ (the input sampling clock) but has different pulse width.
The insertion of data is interrupted after 380 bits have been fed to the serial input register to allow the parallel transfer of charge packets to the parallel registers to occur.

Parallel Registers

Transfer of charge packets through the parallel registers is accomplished by clocking $\emptyset_{V1}$ and $\emptyset_{V2}$, $\emptyset_{H1}$ and $\emptyset_{H2}$ in the same

manner as an imaging device. Data is transferred from the parallel registers to the serial output register by clocking $\emptyset_H$ and $\emptyset_V$.

Serial Output Register

The output register is a 380 element 2 phase analog transport register which transfers the charge packets from the parallel register into the output amplifier. The output register is clocked in the same manner as an imaging device.

Output Amplifier

The two stage floating gate output amplifier is similar to that used in the imaging mode. Figure C-1 illustrates the INPUT/OUTPUT characteristic of the CCD array used as an analog storage device.

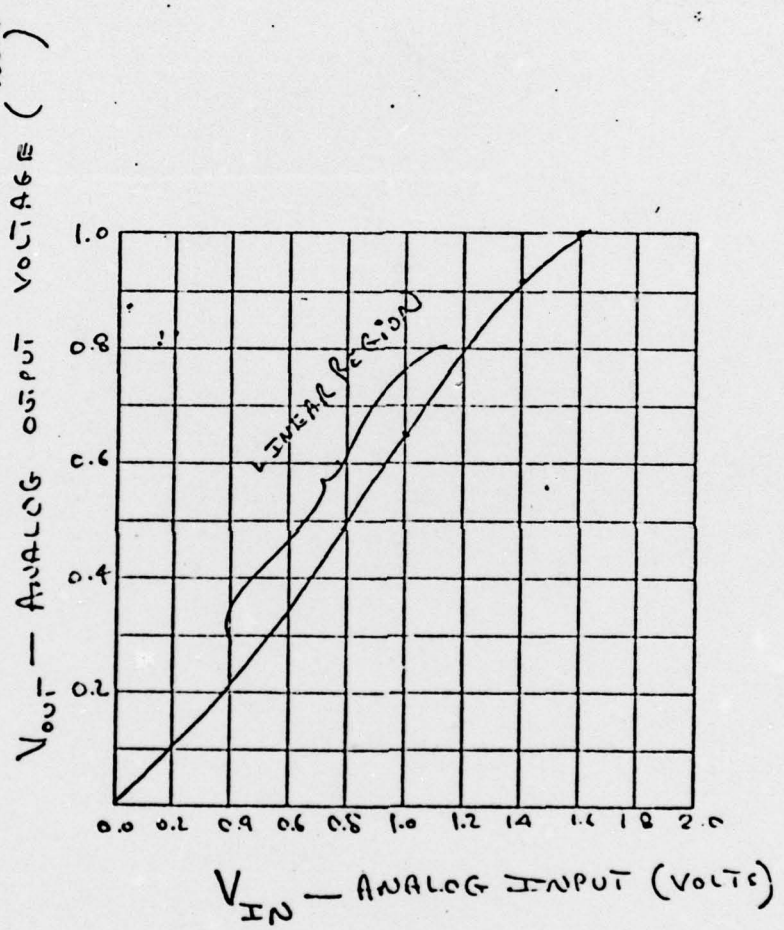


FIGURE C-1. ANALOG STORAGE CCD INPUT/OUTPUT CHARACTERISTICS